

WHAT IS CLAIMED IS:

1 1. A method for storing a digital value to memory in a pipelined instruction
 2 processor, wherein the digital value is read from memory in response to a conditional jump
 3 instruction to determine if the condition of the conditional jump instruction is satisfied, the
 4 method comprising:
 5 generating at least one status bit based on the digital value to be stored, the at least
 6 one status bit indicating if a predetermined condition of a conditional jump instruction is
 7 satisfied; and
 8 storing the digital value and the at least one status bit to memory.

1 2. The method recited in claim 1, wherein the conditional jump instruction
 2 reads the digital value and the at least one status bit from memory to determine if the
 3 condition of the conditional jump instruction is satisfied.

1 3. The method recited in claim 1, wherein the at least one status bit is read
 2 from memory at the same time as the digital value.

1 4. The method recited in claim 1, wherein the memory has one or more
 2 addressable locations, and the at least one status bit is stored at the same addressable
 3 location as the corresponding digital value.

5 status bit generator for generating at least one status bit based on a digital value,
6 the at least one status bit indicating if a predetermined condition of a conditional jump
7 instruction is satisfied; and

8 storing means for storing the digital value and the at least one status bit to the
9 memory.

1 ¹¹
~~10.~~ The pipelined instruction processor recited in claim 9, wherein a selected
2 conditional jump instruction reads the digital value and the at least one status bit from
3 memory to determine if the condition of the conditional jump instruction is satisfied.

1 ¹²
~~11.~~ The pipelined instruction processor recited in claim 9, wherein the at least
2 one status bit is read from the memory at the same time as the digital value is read.

1 ¹³
~~12.~~ The pipelined instruction processor recited in claim 9, wherein the memory
2 has one or more addressable locations, and the at least one status bit is stored at the same
3 addressable location as the corresponding digital value.

1 ¹⁴
~~13.~~ The pipelined instruction processor recited in claim 9, wherein the at least
2 one status bit is set high if the digital value is zero.

1 ¹⁵
~~14.~~ The system recited in claim 9, wherein the at least one status bit is set high
2 if the digital value is a positive value.

1 ¹⁶
~~15.~~ The system recited in claim 9, wherein the at least one status bit is set high
2 if the digital value is negative.

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1 ¹⁷~~16~~ The system recited in claim 9, wherein the at least one status bit is set high
2 if the digital value is a non zero value.

1 ¹⁸~~17~~ The system recited in claim 9, wherein the at least one status bit is set high
2 based on the value of the least significant bit of the digital value.

1 ¹⁹~~18~~ In a pipelined instruction processor that executes instructions including
2 conditional jump instructions, one or more of the conditional jump instructions reading a
3 digital value from memory to determine if the condition of the conditional jump instruction
4 is satisfied, the improvement comprising:
5 a plurality of addressable registers, each of the addressable registers storing a value
6 that includes a digital value and at least one jump status bit;
7 logic to access a current instruction, wherein the current instruction includes an
8 address and a corresponding jump field, the address identifies one of the addressable
9 registers and the corresponding jump field identifies a jump status bit of the at least one
10 jump status bits within the identified addressable register;
11 a jump look-ahead controller for generating a jump look-ahead signal using the
12 address that identifies one of the addressable registers and the jump field that identifies a
13 jump status bit within the identified addressable register, the jump look-ahead signal is a
14 function of the identified jump status bit;

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15 tracking logic for tracking the addresses of a predetermined number of previous
16 instructions in the pipelined instruction processor and comparing the addresses of each
17 previous instruction to the address of the current instruction to generate a series of jump
18 disable signals; and

19 conflict detection logic for generating a jump early signal using the jump look-
20 ahead signal and the series of jump disable signals, the jump early signal initiates the
21 conditional jump depending on the values of the jump disable signals.

1 ²⁰
~~19.~~ The pipelined instruction processor as recited in claim 18, wherein each
2 jump status bit is dependent on the digital value stored in the corresponding addressable
3 register.

1 ²¹
~~20.~~ The pipelined instruction processor as recited in claim 18, further
2 comprising a bit status generator for generating the corresponding jump status bits.

1 ²²
~~21.~~ The pipelined instruction processor as recited in claim 18, further
2 comprising a prediction logic block responsive to the jump early signal for implementing a
3 prediction algorithm to predict the conditional jump depending on the values of the jump
4 disable signals.

1 ²³
~~22.~~ The pipelined instruction processor as recited in claim 18, wherein the
2 tracking logic includes a queue for sequentially storing a pre-determined number of

3 instructions prior to sequentially piping the pre-determined number of instructions through
 4 a read stage and decode stage in a pre-fetch pipeline.

1 ²⁴₂₃ The pipelined instruction processor as recited in claim 22, wherein the pre-
 2 determined number of instructions are sequentially piped through an execution pipeline
 3 after being piped through a pre-fetch pipeline, the execution pipeline includes a write-back
 4 stage.

1 ²⁵₂₄ The pipelined instruction processor as recited in claim 23, wherein the
 2 addressable register is written during the write-back stage.

1 ²⁶₂₅ The pipelined instruction processor as recited in claim 24, wherein the
 2 execution pipeline further includes an address generation stage, a present address stage, an
 3 output operand stage, a capture data stage, and an arithmetic operation stage, all before
 4 the write-back stage.

1 ²⁷₂₆ A method for determine if a condition of a conditional jump instruction is
 2 satisfied in a pipelined instruction processor, the method comprising:
 3 storing a digital value and one or more jump status bits that are based on the
 4 digital value in each of a plurality of address locations in an addressable memory;
 5 accessing a current instruction, the current instruction having an address and a
 6 jump field, the address identifies a selected address location of the addressable memory,

7 and the jump field identifies a selected jump status bit of the selected address location;
8 generating a jump look-ahead signal that is a function of the selected jump status
9 bit read from the selected address location of the addressable memory, the identified jump
10 status bit is accessed using the address and the jump field of the current instruction;
11 tracking the addresses of a predetermined number of previous instructions in the
12 pipelined instruction processor and comparing the addresses to the address of the current
13 instruction to generate a series of jump disable signals; and
14 generating a jump early signal using the jump-look ahead signal and the series jump
15 disable signals, the jump early signal initiates a conditional jump depending on the value of
16 the jump disable signals.